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APPLICATION FOR UNITED STATES LETTERS PATENT

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SILICON DEVICE ON Si:C-OI and SGOI AND METHOD OF MANUFACTURE

DESCRIPTION

BACKGROUND OF THE INVENTION

Field of the Invention

The invention generally relates to a semiconductor device and method of manufacture and, more particularly, to a semiconductor device and method of manufacture which imposes tensile and compressive stresses in the device during device fabrication.

Background Description

Mechanical stresses within a semiconductor device substrate can modulate device performance. That is, stresses within a semiconductor device are known to enhance semiconductor device characteristics. Thus, to improve the characteristics of a semiconductor device, tensile and/or compressive stresses are created in the channel of the n-type devices (e.g., nFETs) and/or p-type devices (e.g., pFETs). However, the same stress component, either tensile stress or compressive stress, discriminatively affects the characteristics of an n-type device and a p-type device.

In order to maximize the performance of both nFETs and pFETs within integrated circuit (IC) chips, the stress components should be engineered and applied differently for

nFETs and pFETs. That is, because the type of stress which is beneficial for the performance of an nFET is generally disadvantageous for the performance of the pFET. More particularly, when a device is in tension (e.g., in the direction of current flow in a planar device), the performance characteristics of the nFET are enhanced while the performance characteristics of the pFET are diminished. To selectively create tensile stress in an nFET and compressive stress in a pFET, distinctive processes and different combinations of materials are used.

For example, a trench isolation structure has been proposed for forming the appropriate stresses in the nFETs and pFETs, respectively. When this method is used, the isolation region for the nFET device contains a first isolation material which applies a first type of mechanical stress on the nFET device in a longitudinal direction (e.g., parallel to the direction of current flow) and in a transverse direction (e.g., perpendicular to the direction of current flow). Further, a first isolation region and a second isolation region are provided for the pFET and each of the isolation regions of the pFET device applies a unique mechanical stress on the pFET device in the transverse and longitudinal directions.

Alternatively, liners on gate sidewalls have been proposed to selectively induce the appropriate stresses in the channels of the FET devices (see, Ootsuka et al., IEDM 2000, p.575, for example). By providing liners, the appropriate stress is applied closer to the device than the stress applied as a result of the trench isolation fill technique.

Also, there have been many proposals to improve both nFET and pFET device performance using tensile and compressive stresses, respectively, which include modulating spacer intrinsic stresses and STI (shallow trench isolation) material changes individually for two MOSFETs using masks. Tensilely strained Si on relaxed SiGe has also been proposed as a means to apply this stress. Unfortunately, the tensilely strained Si on relaxed SiGe can apply only biaxial tensile stress on the Si cap as used in stack form. This constrains the regime of Ge% that is useful because of the nature of pFET sensitivity to stress. The nFET performance monotonically improves with biaxial tension; however, the pFET is degraded with biaxial tension until about 3 GPa at which point it begins to improve.

In order to improve both the pFET and nFET simultaneously, the Ge% needs to be high, approximately greater than 25-30% (or equivalent to approximately greater than 3-4 GPa in stress). This level of Ge% is difficult to implement into processes and is not very manufacturable with major issues including surface roughness, process complexity, defect and yield control, to name but a few. Given that a high Ge% is hard to use for the pFET (since it would be detrimental because of the relatively low levels of tension), other methods must be devised to improve the device performance.

Additionally, Si:C is know to grow epitaxially on Si where it is inherently tensile. A 1% C content in the Si:C/Si material stack can cause tensile stress levels in the Si:C on the order of 500 MPa. In comparison, in the SiGe/Si system about 6% is needed to cause a 500 MPa compression. This 1% level of C can be incorporated into Si during epitaxial

growth as shown in Ernst et al., VLSI Symp., 2002, p. 92. In Ernst, the Si/Si:C/Si is in a layered channel for nFETs. However, the Si:C part of the structure is not relaxed. Instead, in Ernst, an unrelaxed Si:C is used as part of the channel, itself, with a very thin Si cap. The problem with this approach is that the mobility is not enhanced, but retarded, depending on the C content, from scattering.

While these methods do provide structures that have tensile stresses being applied to the nFET device and compressive stresses being applied along the longitudinal direction of the pFET device, they may require additional materials and/or more complex processing, and thus, resulting in higher cost. Further, the level of stress that can be applied in these situations is typically moderate (i.e., on the order of 100s of MPa). Thus, it is desired to provide more cost-effective and simplified methods for creating large tensile and compressive stresses in the channels nFETs and pFETs, respectively.

SUMMARY OF THE INVENTION

In a first aspect of the invention, a method of manufacturing a structure includes forming shallow trench isolation (STI) in a substrate and providing a first material and a second material on the substrate. The first material and the second material are mixed into the substrate by a thermal anneal process to form a first island and second island at an nFET region and a pFET region, respectively. A layer of different material is formed on the first island and the second island. The STI relaxes and facilitates the relaxation of the first island and the second island. In an

embodiment, the first material is deposited or grown Ge material and the second material is deposited or grown Si:C or C.

In another aspect, a method of manufacturing a structure includes forming a substrate and shallow trench isolation in the substrate with a first material. A second material over a pFET region and an nFET region is formed, and is then thermally annealed into the substrate to form a first island and a second island of mixed material. A Si layer is grown on the first island in a first region. The Si layer is strained.

In yet another aspect, the method of manufacturing includes forming a substrate and shallow trench isolation of high temperature stable amorphous material, preferably oxide, in the substrate. The method further includes thermally annealing at least one material into the substrate to form a first island and a second island of mixed material and growing a Si layer on at least the first island. The Si layer is strained. In embodiments:

(i) the at least one material is Ge and the first island and the second island is comprised substantially of a mixed material of relaxed SiGe,

(ii) the at least one material is C or Si:C and the first island and the second island is comprised substantially of a mixed material of relaxed Si:C, and

(iii) the at least one material is Ge and Si:C: or C and the first island are comprised substantially of SiGe and the second island is comprised substantially of Si:C.

In another aspect of the invention, a semiconductor structure includes a substrate and a relaxed shallow trench isolation of high temperature stable amorphous material, preferably oxide, formed in the substrate. A first island of thermally annealed mixed material is formed in the substrate at a pFET region and a second island of thermally annealed mixed material is formed in the substrate at an nFET region. A strained Si layer is formed on at least one of the first island and the second island.

BRIEF DESCRIPTION OF THE DRAWINGS

Figures 1 through 6 represent a fabrication process to form an intermediate structure in accordance with the invention;

Figures 7 through 11 represent a fabrication process to form an intermediate structure in accordance with another aspect of the invention; and

Figures 12a and 12b are representative structures of the invention.

DETAILED DESCRIPTION OF

EMBODIMENTS OF THE INVENTION

This invention is directed to a semiconductor device and method of manufacture which provides desired stresses in the nFET channel and the pFET channel of CMOS devices for improved device performance. In one approach, a SiGe island is obtained through thermally mixing deposited Ge material into an SOI thin film. Similarly, a Si:C island is obtained through thermally mixing deposited Si:C or C into the Si or SOI thin film. By using the method of the invention, the required Ge% is not large and thus does not cause defect issues. Also, relaxation of SiGe and/or Si:C islands in the channels of the pFET and nFET, respectively, can be achieved by the invention to thus provide improved performance as compared to blanket (SiGe or Si:C) substrates. This is because, in the implementations of the invention, a high temperature thermal mixing step, for example, is provided such that shallow trench isolation (STI) can relax and facilitate the relaxation of the SiGe and Si:C islands.

Prior to the invention, placement of at least two crystal islands with different relaxed crystal lattice (different dimensions between the atoms) was only feasible by wafer bonding techniques where the islands have a relatively large size; however, in the invention, the methods yield a unique substrate with small crystal islands which have a relaxed but different crystal structure. In one implementation, the nontrivial element of such structure is the use of high temperature stable amorphous material, e.g., SiO_2, between the islands and the crystal on insulator structure. The unique structure with different (crystal) islands allows for the placement of differently strained layers of

optionally different crystals. In a first aspect, the differently strained layers are tensile and compressive Si layers. In another aspect of the invention, the different layers are a tensile Si layer and SiGe layer or a compressive Si layer and Si:C layer.

The invention has a seminal and important contribution to the art of making substrates with islands on insulator with multiple crystal lattice constants. In the invention, for example, a first island (crystal 1) has a lattice constant $a \geq aSi$ and the second island (crystal 2) has a lattice constant $a \leq aSi$. In one aspect of the invention, as discussed in greater detail below, a Si epitaxial layer of the invention can be selectively grown, which will strain tensilely and compressively on SiGe and Si:C, respectively. This particular application is suitable, for example, in strained planar nFETs and pFETs.

Additionally, it should be understood that holes are known to have excellent mobility in SiGe, but reliable thermal based oxides are hard to form on this material. However, in one implementation of the invention, a dielectric, high K material, for example, is deposited, such that it is possible to use only relaxed SiGe (crystal 1) for the pFET in tandem with crystal 1 (again relaxed SiGe) with the tensilely strained Si for the nFET. It is also contemplated by the invention to use Si:C with compressively stressed Si for the pFET. Thus, the invention is capable of generalizing to the concept of multiple lattice constant islanded substrates.

Referring now to Figure 1, a silicon wafer is shown. Such wafers are commercially available starting substrates for various discrete and integrated circuit (IC) semiconductor device applications. In one implementation, silicon on glass (SOI) wafer

may be fabricated using the SIMOX (Separation by IMplanted OXygen) process, which employs high dose ion implantation of oxygen and high temperature annealing to form a BOX layer in a bulk wafer. As another example, the wafer can be fabricated by bonding a device quality silicon wafer to another silicon wafer (the substrate layer) that has an oxide layer on its surface. The pair is then split apart, using a process that leaves a thin (relative to the thickness of the starting wafer), device-quality layer of single crystal silicon on top of the oxide layer (which has now become the BOX) on the substrate layer. The SOI wafer may also be formed using other processes.

Still referring to Figure 1, an Si layer 20 is formed and patterned to form shallow trench isolation (STI) 25 using standard techniques of pad oxidation, pad nitride deposition, lithography based patterning, reactive ion etching (RIE) of the stack consisting of nitride, oxide, and silicon down to the buried oxide, edge oxidation, liner deposition, fill deposition, and chemical mechanical polish. The STI formation process is well known in the art. In one implementation, high temperature stable amorphous material, e.g., SiO_2, is used for the STI.

Referring to Figure 2, an epitaxial Ge material (layer) 30 is deposited over the surface of the structure using conventional techniques such as chemical vapor deposition methods. For example, ultrahigh vacuum chemical vapor deposition (UHVCVD) may be used in a conventional manner to deposit the Ge layer 30. Other conventional techniques include rapid thermal chemical vapor deposition (RTCVD), limited reaction processing CVD (LRPCVD) and molecular beam epitaxy (MBE). In one embodiment, the thickness of the Ge material may range from 5 to 50 nanometers, or other dimension depending on

the thickness of the underlying Si layer which may, for example, range from 30 to 100 nanometers.

An nFET hard mask 35 is provided on a portion of the Ge layer 30 (e.g., at locations of a yet to be formed nFET device). The nFET hard mask 35 may be a nitride hard mask formed using a conventional deposition process such as spin-on coating, CVD, plasma-assisted CVD, ultrahigh vacuum chemical vapor deposition (UHVCVD), rapid thermal chemical vapor deposition (RTCVD), limited reaction processing CVD (LRPCVD) and other like deposition processes.

In Figure 3, the exposed Ge layer 30 is etched and the nFET mask 35 is stripped using techniques known in the art. For example, the Ge layer 30 may be selectively etched using RIE, wet or dry etching.

As shown in Figure 4, a Si:C material 40 (or optionally C) is deposited on the structure, including over the epitaxially deposited Ge material 35. For example, ultrahigh vacuum chemical vapor deposition (UHVCVD) may be used in a conventional manner to deposit the Si:C (or optionally C) material 40. Other conventional techniques include rapid thermal chemical vapor deposition (RTCVD), limited reaction processing CVD (LRPCVD) and other like processes. In one embodiment, the thickness of the Si:C or C material may range from 5 to 50 nanometers, or other dimension depending on the thickness of the underlying Si layer which may, for example, range from 30 to 100 nanometers. In another aspect, when using C, the thickness may range from 1 to 30 nanometers.

A pFET hard mask 45 is provided on a portion of the Si:C material 40 at locations of the yet to be formed pFET. The pFET hard mask 45 may be a nitride hard mask formed using a conventional deposition process such as spin-on coating, CVD, plasma-assisted CVD, ultrahigh vacuum chemical vapor deposition (UHVCVD), rapid thermal chemical vapor deposition (RTCVD), limited reaction processing CVD (LRPCVD) and other like deposition processes.

As shown in Figure 5, the exposed Si:C layer 40 is then etched and the pFET mask 45 is stripped using techniques known in the art. For example, the Si:C and pFET may be etched using standard etching techniques such as, for example, RIE, wet or dry etching and the like.

In Figure 6, the structure then undergoes a thermal annealing process. During this process, for the nFET device, the deposited Ge material 30 is mixed into the underlying SOI film to form an island 50 of substantially SiGe material. Similarly, in this process, for the pFET, the deposited Si:C or optional C material is mixed into the underlying SOI film forming an island 55 of substantially Si:C material. The thermal annealing process takes place, for example, at about 1200°C to 1350°C between 1 hour and 10 hours, with one implementation at 1200°C for approximately 5 hours.

By using the method of the invention, the required Ge% is not large (e.g., less than 25% and in one implementation 10 to 20%) for the nFET and thus does not cause defect issues. Also, due to the high temperature thermal mixing step, for example, the STI 25 can relax and facilitate the relaxation of the SiGe island 50 and Si:C island 55.

This is due, in part, because the STI comprises oxide material, which is a viscous material at the high temperature, e.g., becomes a low viscosity material at high temperature.

Also, it should now be understood that the SiGe island 50 and the Si:C island 55 have different relaxed crystal lattice (different dimensions between the atoms) which yield a unique substrate with small crystal islands. The relaxation of the SiGe island 50 and the Si:C island 55 provides improved performance as compared to blanket (SiGe or Si:C) substrates. In an implementation, high temperature stable amorphous material, e.g., SiO_2, between the SiGe island 50 and the Si:C island 55 and the crystal on insulator structure are thus used in accordance with the invention.

As further shown in Figure 6, a Si epitaxial layer 60 is selectively grown on the SiGe island 50 and the Si:C island 55 by known processes. In one aspect of the invention, the selectively grown Si epitaxial layer 60 will strain tensilely and compressively on the SiGe island and the Si:C island, respectively. The Si layer 60 may range in thickness, for example, between 5 and 20 nanometers. As with all dimensions and the like, it is contemplated that other dimensions, temperatures, etc. may be used with the invention depending on, for example, the thickness of the underlying substrate.

Now, in implementation, the SiGe island 50 has a lattice constant $a \geq aSi$ and the Si:C island 55 has a lattice constant $a \leq aSi$. That is, standing alone, the Si normally has a lower lattice constant than the SiGe layer; namely, the lattice constant of the Si material does not match the lattice constant of the SiGe layer. However, in the structure of the invention, the lattice structure of the Si layer will tend to match the lattice structure of the

SiGe island. Thus, by virtue of the lattice matching of the Si (which normally is smaller) to the SiGe layer, the Si layer is placed under a tensile stress. This area will act as a strained channel for the nFET. In one embodiment, the Ge content of the SiGe layer may be less than 25% in ratio to the Si content.

Also, standing alone, Si would normally have a larger lattice constant than the Si:C island. That is, the lattice constant of the Si material does not match the lattice constant of the Si:C. However, in the structure of the invention, the lattice structure of the Si layer will tend to match the lattice structure of the Si:C . By virtue of the lattice matching of the Si (which normally is larger) to the Si:C island, the Si layer is placed under a compressive stress. That is, similar to the occurrence with the SiGe, the surrounding areas of the Si:C island will try to obtain an equilibrium state thus resulting in a compressive stress of an epitaxial Si layer formed on the Si:C island. This area will act as a strained channel for the pFET. In one embodiment, as deposited, the C content may be from about up to 4% in ratio to the Si content.

Figures 7-11 show another aspect of the invention. In Figure 7, a silicon wafer such as SOI is shown. As in the previously described structure, the SOI may be fabricated using the SIMOX process or other well known processes. An Si layer 20 is patterned to form shallow trench isolation (STI) 25 using standard techniques of pad oxidation, pad nitride deposition, lithography based patterning, reactive ion etching (RIE) of the stack consisting of nitride, oxide, and silicon down to the buried oxide, edge oxidation, liner deposition, fill deposition, and chemical mechanical polish. The STI formation process is well known in the art.

Referring to Figure 8, a pFET mask 40 is provided on a portion of the structure at locations of the yet to be formed pFET. The pFET hard mask may be deposited using convention techniques such as chemical vapor deposition methods. For example, such techniques may include spin-on coating, CVD, plasma-assisted CVD, evaporation ultrahigh vacuum chemical vapor deposition (UHVCVD), rapid thermal chemical vapor deposition (RTCVD), limited reaction processing CVD (LRPCVD) and other like deposition processes.

An epitaxial Ge layer 30 is selectively grown over the exposed surface of the yet to be formed nFET using conventional techniques. In one embodiment, the thickness of the Ge material may range from 5 to 50 nanometers, or other dimension depending on the thickness of the underlying Si layer which may, for example, range from 30 to 100 nanometers. The hard mask 45 is stripped using well known processes, as discussed above.

In Figure 9, an nFET mask 35 is provided on a portion of the structure at locations of the yet to be formed nFET. The nFET hard mask may be deposited using conventional techniques such as chemical vapor deposition methods as discussed throughout and which should be known to those of ordinary skill.

An Si:C layer 40 is selectively grown over the exposed surface of the structure at the yet to be formed pFET using conventional techniques such as chemical vapor deposition method, as discussed above. In one embodiment, the thickness of the Si:C material may range from 5 to 50 nanometers, or other dimension depending on the

thickness of the underlying Si layer which may, for example, range from 30 to 100 nanometers. The C may even be thinner ranging from 1 to 50 nanometers.

As shown in Figure 10, the nFET hard mask 35 is then removed using well known processes. The structure then undergoes a thermal annealing process. During the annealing process, for the nFET device, the Ge material 30 is mixed into the SOI film forming an island 50 of substantially SiGe material. Similarly, for the pFET, the Si:C or optionally C material is mixed into the SOI film forming an island 55 of substantially Si:C material. This process also forms a BOX layer, as the substrate. The thermal annealing process takes place, for example, at about 1200°C to 1350°C between 1 hour and 10 hours, with one implementation at 1200°C for approximately 5 hours.

As discussed above, and similar to the previous implementations, by using the method of the invention, the required Ge% is not large (e.g., less than 25% and in one implementation from 10 to 20%) and thus does not cause defect issues. Also, due to the high temperature thermal mixing, for example, the STI 25 can relax and facilitate the relaxation of the SiGe island 50 and Si:C island 55. As previously discussed, the relaxation of SiGe and Si:C provides improved performance as compared to blanket (SiGe or Si:C) substrates. In one implementation of the invention, the element of such structure is the use of high temperature stable amorphous material, e.g., SiO_2, between the islands and the crystal on insulator structure.

As further shown in Figure 11, Si epitaxial material 60 is selectively grown on the SiGe island 50 and Si:C island 55. The Si layer 60 may range in thickness, for example,

between 5 and 20 nanometers. In this aspect of the invention, the different layers become a tensile Si layer or a compressive Si layer. The tensile Si layer will act as a strained channel for the nFET and the compressive Si layer will act as a strained channel for the pFET.

In another aspect of the invention, C can be implanted at high dose into the pFET region which can produce concentrations much greater than the 1-4% C in the Si:C upon thermal annealing. The dose may be about 1 e 16 #/cm^2 or greater such as 5 e 16 #/cm^2 .

In the illustrative example of Figure 12a, in one implementation, SiGe may be used for both the nFET and the pFET, excluding Si:C or C. In this implementation, a strained Si will be placed on the nFET region but not on the pFET region. Upon fabrication, the nFET will then be in a tensile stress. A high K dielectric 100, though, to begin the fabrication process of the device, is then selectively grown on the structure; that is, the high K dielectric 100 may be grown over the strained Si layer and the exposed SiGe layer. The high K dielectric 100 may be zirconium oxide or aluminum oxide, for example.

Alternatively, Si:C may be used for both the nFET and the pFET, excluding SiGe. In this implementation, a strained Si will be placed on the pFET region but not on the nFET region. Upon fabrication, the pFET will then be in a compressive stress. A high K dielectric 100, though, to begin the fabrication of the device, is then selectively grown on the structure; that is, the high K dielectric 100 may be grown over the strained Si layer and the exposed Si:C layer. The high K dielectric 100 may be zirconium oxide or

aluminum oxide, for example. This is also representative of Figure 12b. The processes for using Si:C or SiGe remain the same, as discussed above.

The structures formed, as shown in Figure 6, Figure 11 and Figures 12a and 12b, are intermediate structures that accommodate formation of semiconductor devices, such as pFETs and nFETs, in accordance with the principles of the invention. To form the final device, standard CMOS processes may be performed to form devices such as field effect transistors on the structure, as is well known in the art. For example, the devices may include ion implantation of source and drain regions separated by the semi-conducting channel of strained Si (or Si and SiGe and Si and Si:C). That is, the nFET will be formed over the tensilely strained Si channel and the pFET will be formed over the compressively strained Si channel. A gate oxide is provided atop the strained Si channel, and a gate conductor is provided on top of the gate oxide. Spacers are also provided. These components are found in typical field effect transistors and further explanation is not needed for one of ordinary skill in the art to readily understand the fabrication process of the FET device.

While the invention has been described in terms of embodiments, those skilled in the art will recognize that the invention can be practiced with modification within the spirit and scope of the appended claims. For example, the invention can be readily applicable to bulk substrates.